

CLAIMS

What is claimed is:

1 1. A current sense circuit comprising:
2 first and second transistors, each having first and
3 second terminals and a control terminal, the conduction
4 through each transistor between the first and second
5 terminals being controlled by the voltage between the control
6 terminal and the first terminal of the respective transistor;
7 the first transistor having its first and second
8 terminals configured to connect in series with a first power
9 supply terminal and a load;
10 the first terminal of the second transistor being
11 connected to the first terminal of the first transistor, and
12 the control terminal of the second transistor being connected
13 to the control terminal of the first transistor;
14 first biasing circuitry biasing the first and second
15 transistors to operate with equal first to second terminal
16 voltages;
17 a first control loop responsive to a reference voltage
18 to clamp the first to second terminal voltages of the first
19 and second transistors to a predetermined voltage; and,
20 a second control loop providing a sense circuit output
21 current linearly varying with the current through the second
22 transistor.

1 2. The current sense circuit of claim 1 where the
2 second control loop has a high output impedance.

1 3. The current sense circuit of claim 1 wherein the
2 first transistor is N times larger than the second
3 transistor, wherein N is substantially greater than one.

1 4. The current sense circuit of claim 3 wherein the
2 second control loop provides a sense circuit output current
3 component equal to the current through the second transistor
4 minus a bias current on the second transistor.

1 5. The current sense circuit of claim 4 further
2 comprised of second biasing circuitry biasing the sense
3 circuit output current to a zero current when a load current
4 is zero.

1 6. The current sense circuit of claim 1 wherein the
2 second control loop is not active when the voltage on the
3 load connection to the first transistor approaches the
4 voltage of a second power supply terminal, and further
5 comprising a third control loop, the third control loop
6 providing a sense circuit output current linearly varying
7 with the current through the second transistor when the
8 voltage on the load connection to the first transistor
9 approaches the voltage of a second power supply terminal.

1 7. The current sense circuit of claim 6 further
2 comprising:
3 a second current sense circuit comprising:
4 third and fourth transistors, each having first and
5 second terminals and a control terminal, the conduction
6 through each transistor between the first and second
7 terminals being controlled by the voltage between the
8 control terminal and the first terminal of the
9 respective transistor;
10 the third transistor having its first and second
11 terminals configured to connect in series with a second
12 power supply terminal and a load;
13 the first terminal of the fourth transistor being
14 connected to the first terminal of the third transistor,
15 and the control terminal of the fourth transistor being
16 connected to the control terminal of the third
17 transistor;
18 first biasing circuitry biasing the third and
19 fourth transistors to operate with equal first to second
20 terminal voltages;
21 a first control loop responsive to a reference
22 voltage to clamp the first to second terminal voltages
23 of the third and fourth transistors to a predetermined
24 voltage; and,

25 a second control loop providing a sense circuit
26 output current linearly varying with the current through
27 the fourth transistor; and,
28 a third current sense circuit comprising:
29 fifth and sixth transistors, each having first and
30 second terminals and a control terminal, the conduction
31 through each transistor between the first and second
32 terminals being controlled by the voltage between the
33 control terminal and the first terminal of the
34 respective transistor;
35 the fifth transistor having its first and second
36 terminals configured to connect in series with a first
37 power supply terminal and a load;
38 the first terminal of the sixth transistor being
39 connected to the first terminal of the fifth transistor,
40 and the control terminal of the sixth transistor being
41 connected to the control terminal of the fifth
42 transistor;
43 first biasing circuitry biasing the fifth and sixth
44 transistors to operate with equal first to second
45 terminal voltages;
46 a first control loop responsive to a reference
47 voltage to clamp the first to second terminal voltages
48 of the fifth and sixth transistors to a predetermined
49 voltage; and,

50 a second control loop providing a sense circuit
51 output current linearly varying with the current through
52 the second transistor;
53 the output of the current sense circuit of claim 5 being
54 coupled to flow between the first and second terminals of the
55 third transistor, the output of the second current sense
56 circuit being coupled to flow between the first and second
57 terminals of the third current sense output.

1 8. The current sense circuit of claim 7 wherein the
2 first power supply terminal is a positive power supply
3 terminal and the second power supply terminal is a negative
4 power supply terminal relative to the positive power supply
5 terminal.

1 9. The current sense circuit of claim 7 further
2 comprised of a resistor coupled to the output of the third
3 current sense circuit output.

1 10. A current sense system operating between first and
2 second power supply terminals comprising:
3 a first current sense circuit coupled between the first
4 and second power supply terminals and having a first current
5 sense input and a first current sense output, the first
6 current sense circuit providing a current sense output
7 current proportional to the current in the first current

8 sense input when the voltage on the first current sense input
9 is between the voltages on the first and second power
10 supplies;

11 a second current sense circuit coupled between the first
12 and second power supply terminals and having a second current
13 sense input coupled to the first current sense output, and a
14 second current sense output, the second current sense circuit
15 providing a second current sense output current proportional
16 to the current in the second current sense input while
17 holding the voltage between the second current sense input
18 and the second power supply terminal constant; and,

19 a third current sense circuit coupled between the first
20 and second power supply terminals and having a third current
21 sense input coupled to the second current sense output, and a
22 third current sense output, the third current sense circuit
23 providing a third current sense output current proportional
24 to the current in the third current sense input while holding
25 the voltage between the second current sense input and the
26 first power supply terminal constant.

1 11. A method of sensing current using transistors, each
2 having first and second terminals and a control terminal, the
3 current flow between the first and second terminals being
4 controlled by the voltage between the control terminal and
5 the first terminal, comprising:

6 coupling the first and second terminals of the first
7 transistor in series with a source of power and a load;
8 using a first control loop responsive to a set voltage,
9 mirroring a current proportional to the current through the
10 first transistor to a second transistor while maintaining the
11 voltages between the control terminal and the first terminal
12 of the first and second transistors equal, and also
13 maintaining the voltages between the first and second
14 terminals of the first and second transistors equal; and,
15 providing a current sense output responsive the current
16 between the first and second terminals of the second
17 transistor.

1 12. The method of claim 11 wherein the current sense
2 output is provided by a second control loop, the second
3 control loop providing a current sense output current
4 changing linearly with and equal to changes in current
5 between the first and second terminals of the second
6 transistor.

1 13. The method of claim 12 further comprised of
2 including a bias current in the current sense output current
3 to make the current sense output current equal to zero when
4 the load current is zero.

1 14. A method of current sensing comprising:
2 passing the current to be sensed through a transistor;
3 controlling the transistor so that the voltage drop
4 across the transistor is independent of the current to be
5 sensed; and,
6 providing an output responsive to the current in the
7 transistor.

1 15. The method of claim 14 wherein the output is
2 proportional to the current in the transistor.

1 16. The method of claim 15 wherein the output is a
2 current.

1 17. The method of claim 14 further including
2 replicating the current in the transistor to provide a
3 replica current proportional to the current in the
4 transistor, and wherein providing an output responsive to the
5 current in the transistor comprises providing an output
6 responsive to the replica current.

1 18. The method of claim 14 wherein the transistor is a
2 FET.

1 19. A method of current sensing comprising:
2 providing first and second transistors, the first
3 transistor being N times the size of the second transistor;
4 passing the current to be sensed through the first
5 transistor;
6 controlling the first and second transistors so that the
7 voltages across the first and second transistors are equal to
8 a reference voltage and independent of the input current to
9 replicate the current in the first transistor in the second
10 transistor in a ratio of $1/N$; and,
11 providing an output that varies linearly with the
12 current in the second transistor.

1 20. The method of claim 19 wherein the first and second
2 transistors are biased by bias current sources.